What is claimed is:

1. A method of passivating a silicon nitride spacer comprising the steps of:

providing a semiconductor substrate having a horizontal surface;

forming source and drain regions in the surface of the substrate;

forming a gate electrode on the horizontal surface of the substrate between said source and drain regions, said gate electrode having a horizontal top surface and sidewalls;

providing silicon nitride spacers on the sidewalls of the gate electrode;

depositing a thin layer of silicon oxide over silicon nitride spacers and said horizontal surface of said semiconductor substrate and the horizontal top surface of said gate electrode;

removing the silicon oxide layer over said horizontal surface of said semiconductor substrate and the horizontal top surface of said gate electrode;

depositing nickel on said horizontal top surface of said gate and the horizontal surface of the substrate; and

annealing to react the nickel with silicon in the horizontal top surface of the gate electrode and in the horizontal surface of the substrate to form a metal silicide on said horizontal surfaces.

2. The method of claim 1, wherein said silicon oxide is formed by treating said substrate in a mixture of sulfuric acid and hydrogen peroxide.

3. The method of claim 1, wherein the gate dielectric is a dielectric selected from the group consisting of silicon dioxide, silicon oxynitride or a high-K dielectric.

4. The method of claim 1, where in the thickness of the silicon oxide layer is 20 Å.

5. The method of claim 4, wherein the thickness of the silicon oxide layer is 20 Å.

6. The method of claim 5, wherein the silicon oxide is removed using anisotropic sputter etching.

7. The method of claim 1 which includes the further step of removing the unreacted nickel.

8. A semiconductor device comprising:

a semiconductor substrate having a horizontal surface;

source and drain regions in the surface of the substrate;

a gate electrode on the horizontal surface of the substrate between said source and drain regions, said gate electrode having a horizontal top surface and sidewalls;

silicon nitride spacers on the sidewalls of the gate electrode;

a thin layer of silicon oxide over silicon nitride spacers; and

a nickel silicide on said horizontal surfaces.